Claims

What is claimed is:

1. An integrated circuit comprising:

a plurality of standard cells; and

a plurality of spare gates interspersed with the standard cells;

the plurality of spare gates being arranged in multiple groups of spare gates, at least a given one of the groups of spare gates being arranged between first and second rows of the standard cells.

2. The integrated circuit of claim 1 wherein at least the given one of the groups of spare gates comprises an *m* x *n* array of spare gate cells arranged between the first and second rows of the standard cells, where both *m* and *n* are greater than one, each of at least a subset of the spare gates in the given group comprising a plurality of base transistor structures.

3. The integrated circuit of claim 1 wherein the multiple groups of spare gates are configured as a plurality of spare gate islands distributed throughout a standard cell portion of the integrated circuit, with one or more of the spare gate islands comprising an array of spare gate cells arranged between rows of the standard cells.

4. The integrated circuit of claim 1 wherein a total number of the spare gate groups is greater than or equal to four.

5. The integrated circuit of claim 1 wherein at least one of the spare gates comprises a spare gate diode cell.

6. An integrated circuit comprising:

a plurality of standard cells; and

a plurality of spare gates interspersed with the standard cells in a substantially uniform manner.

7. The integrated circuit of claim 6, wherein the spare gates are interspersed with the standard cells in accordance with a predetermined geometric pattern.

8. The integrated circuit of claim 6 wherein at least one of the spare gates is convertible to an active logic gate using connections formed in one or more metallization layers of the integrated circuit.

9. The integrated circuit of claim 6 wherein the spare gates of the integrated circuit are each formed using one or more base transistor structures and the standard cells are not formed using the base transistor structures.

10. The integrated circuit of claim 6 wherein each of at least a subset of the spare gates comprises a spare gate cell implemented using one or more base transistor structures.

11. The integrated circuit of claim 10 wherein the base transistor structure comprises:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end extending past another of the source and drain regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis.

12. The integrated circuit of claim 6, wherein the plurality of spare gates are configured as spare gate islands distributed among a standard cell portion of the integrated circuit.

13. A method of designing an integrated circuit, comprising:

providing a plurality of standard cells;

providing a plurality of spare gates; and

interspersing the plurality of spare gates with the standard cells in a substantially uniform manner.

14. The method of claim 13, wherein interspersing the plurality of spare gates with the standard cells comprises arranging the plurality of spare gates in multiple groups, at least a given one of the groups of spare gates being arranged between first and second rows of the standard cells.

15. The method of claim 13, wherein the spare gates are interspersed with the standard cells in accordance with a predetermined geometric pattern.

16. The integrated circuit of claim 13, wherein at least a portion of the standard cells and spare gates are interspersed in accordance with a placement operation of an automated place and route process of a standard cell design tool.

17. The integrated circuit of claim 13 including defining an area within the integrated circuit for the spare gates using a floorplan operation of a standard cell design tool.

18. An article of manufacture on which is stored a computer program for use in designing an integrated circuit, wherein the program when executed implements the following method:

providing a plurality of standard cells;

providing a plurality of spare gates; and

interspersing the plurality of spare gates with the standard cells in a substantially uniform manner.

19. The article of manufacture of claim 18, wherein interspersing the plurality of spare gates with the standard cells comprises arranging the plurality of spare gates in multiple groups, at least a given one of the groups of spare gates being arranged between first and second rows of the standard cells.

20. The article of manufacture of claim 18, wherein the spare gates are interspersed with the standard cells in accordance with a predetermined geometric pattern.